

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re The Application of:
Peter Szpak et al.

Serial No.: 10/759,346

Filed: January 15, 2004

For: A SYSTEM AND METHOD FOR
SCHEDULING THE EXECUTION OF
MODEL COMPONENTS USING
MODEL EVENTS

Examiner: Ke, Peng

Art Unit: 2174

Confirmation No.: 7444

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May 16, 2011

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Sir:

REPLY BRIEF

In response to the Examiner's Answer mailed March 15, 2011, Applicant submits
this Reply Brief. This Reply Brief is being submitted in accordance with 37 C.F.R.

§41.41.

I. STATUS OF CLAIMS

Claims 1-29 and 33-61 are pending.

Claims 1-29 and 33-61 stand finally rejected under 35 U.S.C. §103, as set forth in the final Office Action mailed March 30, 2010.

The rejection of claims 1-29 and 33-61 is appealed.

II. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether independent claims 1, 19, 33, and 51, which satisfy all other conditions of patentability, are unpatentable under 35 U.S.C. §103 on the grounds that they are obvious based on U.S. Patent No. 7,134,109 to Hayles (“Hayles”) in view of U.S. Patent No. 5,522,073 to Courant et al. (“Courant”) and U.S. Patent No. 6,880,130 to Makowski et al. (“Makowski”).

Whether claims 4 and 36, which satisfy all other conditions of patentability, are unpatentable under 35 U.S.C. §103 on the grounds that they are obvious based on Hayles in view of Courant and Makowski.

Whether claims 14 and 46, which satisfy all other conditions of patentability, are unpatentable under 35 U.S.C. §103 on the grounds that they are obvious based on Hayles in view of Courant and Makowski.

Whether claims 20 and 52, which satisfy all other conditions of patentability, are unpatentable under 35 U.S.C. §103 on the grounds that they are obvious based on Hayles in view of Courant and Makowski.

Whether claims 28 and 60, which satisfy all other conditions of patentability, are unpatentable under 35 U.S.C. §103 on the grounds that they are obvious based on Hayles in view of Courant and Makowski.

III. ARGUMENT

This Reply Brief addresses three issues raised in the Examiner's Answer. The Board of Patent Appeals and Interferences is directed to Applicant's Appeal Brief for a further discussion of the issues on appeal.

A. Hayles' Fig. 8 is not an Executable Graphical Model of Time-Based Components, as Claimed.

Claim 1 recites in part:

displaying a view of an executable graphical model with a plurality of executable time-based components ...

The Reply Brief, on p. 15, contends that Fig. 8 and other excerpts from Hayles teach the claimed "time-based components". Applicant's Appeal Brief addresses the other excerpts from Hayles. To the extent the Examiner's Answer contends that Fig. 8 discloses "an executable graphical model with a plurality of time-based components", Applicant responds as follows.

Fig. 8 of Hayles is not an executable graphical model. Hayles clearly states that Fig. 8 "is a flowchart diagram of one embodiment of a method for representing and specifying timing and triggering for hardware devices." Hayles, at Col. 17, lines 3-5. That is, Fig. 8 is merely a drawing that illustrates a sequence of steps that can be performed. Hayles' Fig. 8 does not represent a model of a system, such as a dynamic system. Hayles' Fig. 8 is also not executable. The steps of Fig. 8, which are separately enclosed in their own boxes, are not executable time-based components. They are simply the steps of a method that may be performed. For at least these reasons, Hayles' Fig. 8 cannot fairly be equated with the claimed executable time-based components of an executable graphical model.

B. The Cited References Fail to Disclose or Suggest the Claimed “Post Component”.

Claim 1 recites in part:

an executable graphical model ... including at least one user-configurable, executable graphical post component having at least one input port for receiving at least one input signal, said ... post component being configured to post an event when a condition associated with said at least one input signal ... is satisfied.

In response to Applicant’s argument that the cited references fail to disclose or suggest the claimed “user-configurable, executable graphical post component”, the Reply Brief, at p. 15, states that “Hayles teaches posting an input when a specific time is trigger.” This is not, however, what is being claimed. As shown in the above excerpt, claim 1 expressly recites a “user-configurable, executable graphical post component” that is included in an executable graphical model. In other words, the claim clearly recites a particular component of an executable graphical model, namely a user-configurable, executable graphical post component. Claim 1 does not simply claim posting an input, as contended in the Examiner’s Answer. As set out in the Appeal Brief, neither Hayles nor the other references disclose or suggest a user-configurable, executable graphical post component that is included in an executable graphical model.

C. Hayles’ Fails to Disclose or Suggest Interrupting the Execution of an Executing Event.

Independent method claim 19 recites, in part:

displaying ... an executable model with a plurality of executable time-based components, said model including (a) post component having at least one input port for receiving at least one input signal, said ... post component being configured to post a specified event when a condition associated with said ... input signal ... is satisfied

interrupting execution of an executing event in response to said posting of said specified event; and

performing an operation in said executable model within said graphical modeling environment in response to said posting of said specified event.

The Examiner's Answer, at p. 17, cites to Hayles at Col. 26, line 40 to Col. 27, line 5 as purportedly teaching the claimed "interrupting execution of an execution event in response to posting of (a) specified event." This excerpt in its entirety states as follows:

In contrast, FIG. 14B illustrates an example diagram for graphically representing and configuring similar Analog Input Triggering for the E Series device, according to one embodiment of the present invention. In the configuration shown, an Analog Edge with hysteresis Start Trigger is configured using the signal at PFI 0 pin as source. The Start trigger is configured to occur on the falling edge of ACE signal. A Digital Edge Reference Trigger is configured to occur on the falling edge of signal at PFI 1 pin and is exported to RTSI 1. In this configuration 1000 pre-trigger samples will be acquired, and pre-trigger sampling is configured to begin after a delay of 0.02 seconds from the Start Trigger occurrence.

Reflecting this addition of a delay of the sampling with respect to the start trigger, the state diagram includes a "Wait for Delay Period to Elapse" node coupled to the Wait for Start Trigger node. More specifically, once an "Arm" software command is received, denoted by the dot-dash transition path, the system will wait for a Start Trigger, as indicated by the solid transition path labeled "Start Trigger", then wait for the specified delay period, at which point the sample acquisition process will occur, as shown. As FIG. 14B also shows, the pre-trigger sampling process is represented by an "Acquire Minimum Pre-Reference Trigger Samples" state node which, after the specified 1000 pre-samples are acquired, transitions to a "Wait for Reference Trigger While Acquiring More Samples" state. When the reference trigger occurs, this system transitions to an "Acquire Post-Reference Trigger Samples" state, where the post-reference trigger samples are acquired. As shown, once the samples are acquired, the idle state resumes.

This excerpt discusses Fig. 14B of Hayles which shows a diagram used to configure an "E series" data acquisition, computer plug-in board. Fig. 14B is intended to be compared with Fig. 14A, which illustrates the prior art approach. As discussed in the

excerpt, the device is configured so that after a Start Trigger occurs, a delay period of 0.02 seconds occurs. During this delay period, 1000 pre-Reference Trigger data samples are acquired by the plug-in board. Then, after the Reference Trigger occurs, more data samples are acquired by the plug-in board. The Examiner's Answer does not identify what parts of the excerpt are being equated with the claimed "post component", "specified event", or "executing event" whose execution is interrupted.

Nevertheless, the cited excerpt provides no disclosure or suggestion of either (i) a post component of an executable model that posts a specified event, or (ii) interrupting execution of an executing event in response to the posting of the specified event. At no point does Hayles identify any part of Fig. 14B as an executable model. Hayles also fails to identify a post component of an executable model. Finally, Hayles makes no mention of a specified event, as posted by a post component, interrupting execution of an executing event. Instead, the cited excerpt describes a sequence of steps, e.g., a Start Trigger, a Delay Period, the Acquisition of pre-Reference Trigger data samples, and the acquisition of post-Reference Trigger Data samples.

CONCLUSION

Applicant respectfully submits that the claims are allowable over the art of record, and requests that the rejection of all claims be reversed.

Please charge any additional fee occasioned by this paper to our Deposit Account
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Respectfully submitted,

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